Features

FW1906 is a six-channel LED fixed constant current drive control circuit, which integrates MCU single-line digital interface, data latch, LED fixed constant current drive, PWM brightness control and other circuits. The chip can be cascaded through the single-line digital interface (DI, DO), and the external controller only needs a single line to control the chip and the subsequent chips cascaded with it. The PWM brightness of the FW1906 output port can be set separately by an external controller.

Features

Power CMOS technology; VCC voltage supports 24V OUT output port

withstand voltage 24V OUT port fixed

constant current 18mA

Brightness adjustment circuit, 256 levels of brightness adjustable

Single-line serial cascade interface

Oscillation mode: built-in RC oscillation and clock synchronization according to the signal on the data line. After receiving the data of this unit, it can automatically regenerate the subsequent data and send it to the next level through the data output terminal. The signal will not be distorted or attenuated as the cascade becomes farther

Built-in power-on reset circuit, white light on when powered on

PWM control terminal can achieve 256-level adjustment, scanning frequency above 2.6KHz Data reception and decoding can be completed through one signal line

When the refresh rate is 30 frames/s, the cascade number is not less than 1024 points

Data transmission rate can reach 800Kbps

The transmission distance between any two points is not less than 20 meters

Package form: SSOP10

Internal structure diagram

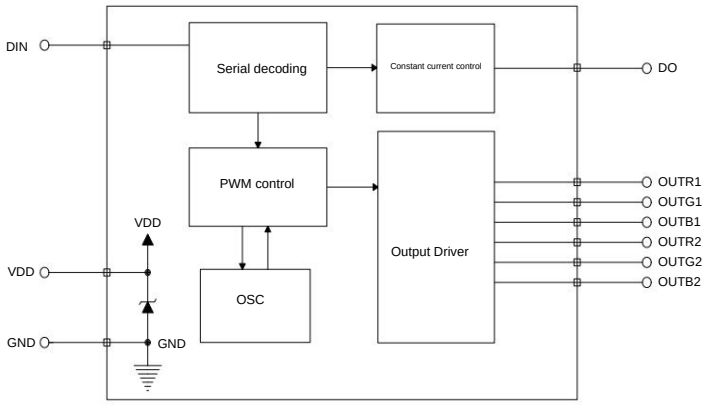

figure 1

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Pin Arrangement

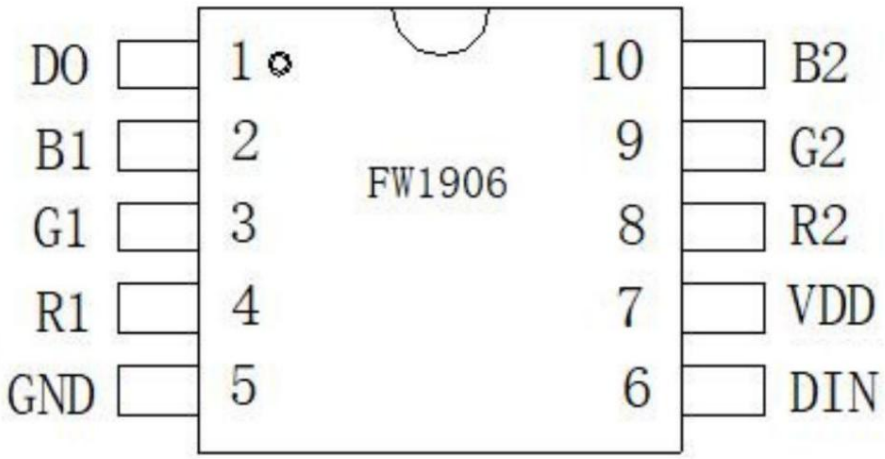

figure 2

Pin Function

Port		I/O	Functional Description
Name Pin			
DIN	6	I	Data Input
DO	1	O	Data output
R1	4	O	Red PWM constant current output
G1	3	O	Green PWM constant current output
B1	2	O	Blue PWM constant current output
R2	8	O	Red PWM constant current output
G2	9	O	Green PWM constant current output
B2	10	O	Blue PWM constant current output
VDD	7	-	Logic power supply
GND	5	-	Connect to system ground

-

Table 1

Output and input equivalent circuit

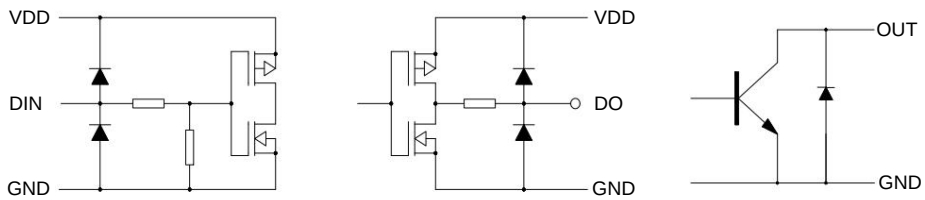

image 3

Integrated circuits are electrostatically sensitive devices. When used in dry seasons or dry environments, they are prone to generate a large amount of static electricity. Static electricity discharge may

It is recommended to take all appropriate precautions for handling the integrated circuit. Improper operation and soldering may damage the integrated circuit.

It will cause ESD damage or performance degradation, and the chip will not work properly.

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(1)(2)

Limit parameters

parameter			scope	unit
VDD	Logic supply voltage		24	V
Vin	Input voltage range	DIN. SET	-0.4-5.5	V
Iout	Output current (DC)	OUTR,OUTG,OUTB	18	mA
Vout	Output voltage range	OUTR,OUTG,OUTB	-0.4-+30.0	V
Fosc	DIN clock rate	DIN	400-900	KHz
Topr	Operating Temperature		-40-+85	℃
Ts	Range Storage Temperature		-55-+150	℃
ESD	Range Human Body Model (HBM)		4000	V

Table 2

(1) The levels in the table above may cause permanent damage to the device and reduce the reliability of the device under long-term use conditions.

We do not recommend operating the chip beyond these extreme parameters under any other conditions;

(2) All voltage values are tested relative to system ground.

Recommended operating conditions range

(At -40℃+85℃, GND=0V) unless otherwise specified			FW1906			unit
Parameters		Test Conditions	Min.	Typ.	Max.	
VDD	Power supply voltage		10	24	27	V
VIN	DIN\SET Input withstand voltage range	VDD=5V, DIN, SET series Connect 1K resistor	-0.5	5	5.5	V
VDO	DO output withstand voltage range	VDD=5V, DO is connected in series with 1K resistor	-0.5	--	5.5	V
VOUT	OUT Output withstand voltage range	OUT=OFF	-0.5	--	24.0	V
TA	Operating temperature range		-40		+85	℃
TJ	Operating junction temperature range		-40		+125	℃

table 3

Electrical characteristics

(At VDD=5.0V and -40℃+85℃, typical values are VDD=5.0V and TA = +25°C) unless otherwise specified			FW1906			unit
Parameters		Test Conditions	Min.	Typ.	Max.	
VIH	High level input voltage	VDD=5.0V	3.5		VDD	V
VIL	Low level input voltage	VDD=5.0V	0		1.35	V
IOH	High level output current	VDD=5.0V,SDO=5.0V		1		mA
IOL	Low level output current	VDD=5.0V,SDO=5.0V		10		mA
Iin	DIN, SET input current DIN, SET	VDD=5.0V,SDO=1.0V	-1		1	μA
Icco	Logic supply current (VDD)	connected to VDD or GND OUTR, OUTG, OUTB, DIN, DO=Open	1.2	3.0	4.2	mA
Iolc	Output Constant output current range	OUTR, OUTG, OUTB = 3.0V		18		mA
TPWM	OUT port duty cycle	OUT is connected to a pull-up resistor	0		0.3	μA
		OUT connected to pull-up resistor	270	280	290	μs
ΔIolc0	constant current error (channel to channel)	OUTR, OUTG, OUTB =ON ,VOUTn =1V			±2.5	%
ΔIolc1	Constant current error (Chip to Chip)	OUTR, OUTG, OUTB =ON ,VOUTn =1V			±5	%

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ΔIolc2	Linear adjustment	OUTR, OUTG, OUTB =ON ,VOUTn =1V		±0.5	±1	%/V
ΔIolc3	Load Regulation	OUTR, OUTG, OUTB =ON ,VOUTn =1V～3V		±1	±3	%/V
IDDdyn	Dynamic current consumption	OUTR, OUTG, OUTB = OFF DO=Open			3	mA
Rth(j-a)	Thermal	--	79.2		190	℃/W
PD	resistance Power consumption	(Ta=25°C)			1.5	W

Table 4

Switching Characteristics

(At VDD=5.0V and -40℃-+85℃, typical value VDD=5.0V and TA=+25℃) Unless otherwise specified

symbol	parameter	Test Conditions	Min	Typ	Max	Unit
Fosc	DIN clock rate	VDD=5.0V	-	800	-	KHz
FOUT	OUT PWM output frequency	OUTR, OUTG, OUTB	2.2	2.6	3.2	KHz
tPLZ	Transmission delay time	DIN → DOUT			300	ns
tPZL		CL = 15pF, RL = 10K Ω			100	ns
TZ	Fall time	CL =300pF. OUTR.OUTG. OUTB			80	μs
CI	Input Capacitance	--			15	pF

table 5

Timing characteristics

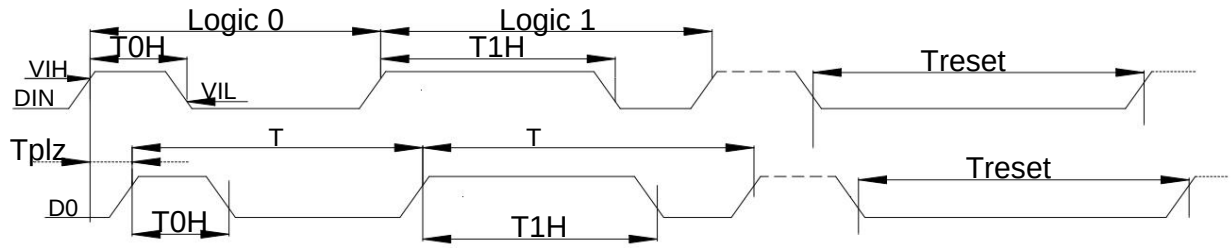

Figure 4

Function Description

This chip uses a single-line communication method and uses the return-to-zero code method to send signals. After the chip is powered on and reset, it receives the signal sent from the DIN terminal. After receiving 24×2 bits of data, the DO port starts forwarding the data sent by the DIN port, providing input data for the next cascade chip.

Before forwarding data, the DO port is always at a low level. If the DIN inputs the RESET signal, the chip will receive 24

×2bit data output corresponds to the PWM duty cycle, and the chip waits for new data again. After receiving the initial 24×2bit data,

Data is forwarded through the DO port. Before the chip receives the RESET signal, the original outputs of the OUTR, OUTG, and OUTB pins remain unchanged.

The chip adopts automatic shaping and forwarding technology, and the signal will not be distorted or attenuated, so that the number of cascades of the chip is not limited by signal transmission. Limited by the screen refresh speed requirement.

data structure

PWM mode commands:

If it is in a 24-bit data packet, the data packet is PWM setting data, and its structure is as follows:

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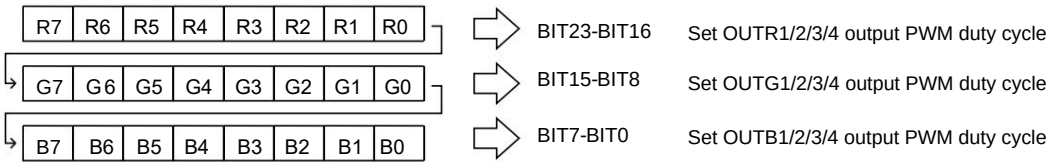

The above is the data format for setting the first group of RGB PWM. To set a FW1906, two groups of data packets with the same format are required.

The PWM duty cycle is continuously adjustable from 0 to 256. When sending 24×2bit data, the high bit is sent first and the data is sent in the order of RGB. Split into three 8-bit data to send. Note that the low level time between bytes should not exceed the RESET signal time, otherwise the chip will reset. If the bit is reset and data is received again, data transmission cannot be achieved.

Communication rate

Symbolic parameters		Test Conditions	Min.	Typ.	Max.	Unit
T0H	Input 0 code, high level time	VDD=5V GND=0V	320	360	400	ns
T1H	Input 1 code, high level time		640	720	800	ns
T0H'	Output 0 code, high level time		--	360	--	ns
T1H'	Output 1 code, high level time		--	720	--	ns
T	0 code or 1 code cycle time		--	1250	--	ns
T reset	Reset code, low level time		200	500		μs

Table 6

Note: The typical cycle time for sending a 1 or 0 code is 1250ns (frequency 800KHz).

Data transmission and forwarding

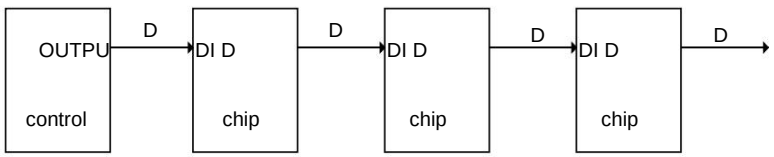

Figure 5

D1 is the data sent by the controller, and D2, D3, and D4 are the data forwarded by the cascaded FW1906.

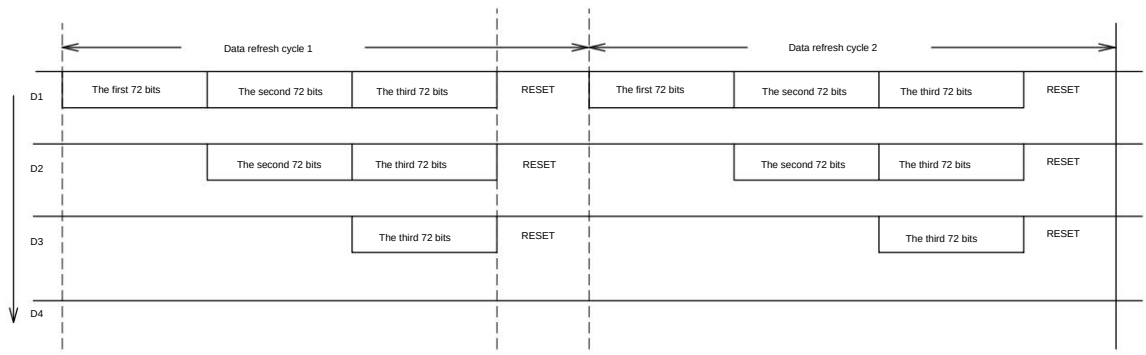

Figure 6

Chip cascading and data transmission and forwarding process: The controller sends data (D1). When chip 1 receives the first 48 bits, chip 1 has not yet There is forwarded data (D2), and then the controller continues to send data, and chip 1 receives the second 48 bits. Since chip 1 already stores the first 48 bits, Therefore, chip 1 forwards the second 48 bits through DO, and chip 2 receives the data (D2) forwarded by chip 1. At this time, chip 2 has not yet forwarded the second 48 bits. Send data (D3); the controller continues to send data, and chip 1 forwards the third 48 bits received to chip 2. Since chip 2 also has There is a 48-bit, so chip 2 forwards the third 48-bit (D3), and chip 3 receives the third 48-bit. At this time, if the controller sends a

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When a RESET low level signal is sent, all chips will reset and decode the 48-bit data received by each chip to control the output of four groups of RGB ports, completing a data refresh cycle. The chip returns to the receiving ready state.

Application Information

1. How to calculate the data refresh rate

The data refresh time is calculated based on how many pixels are cascaded in a system. A set of RGB is usually one pixel (or one segment).

One FW1906 chip can control two groups of RGB.

According to the normal mode

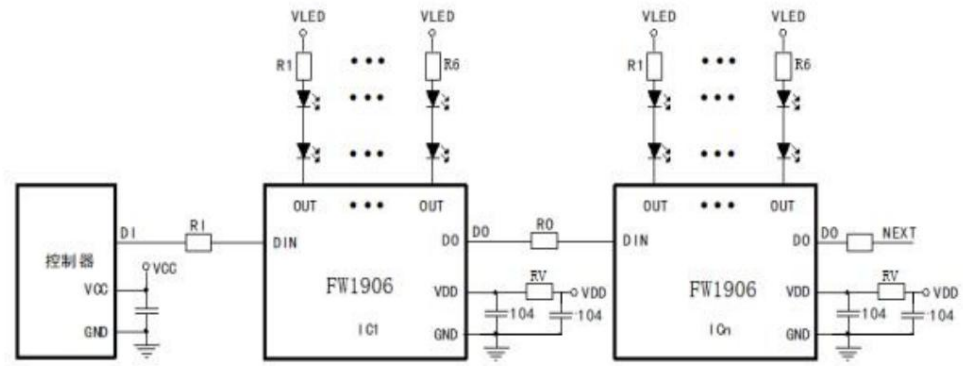
calculation: The maximum transmission rate of one BIT is 1200ns (frequency 800KHz), one pixel data includes red (8BIT), green (8BIT), blue (8BIT) 24BIT bits in total, the transmission time is 24×1.2uS=28.8uS, if there are 2000 pixels in a system, the time to refresh all the displays at one time is 28.8uS×2000=57.6mS (ignoring the RESET code time), that is, the refresh rate for one second is: 1÷57.6×1000=17.36Hz. The following is the table of the maximum data refresh rate corresponding to the number of cascade points:

	Normal	
pixel	mode fastest data refresh time	Maximum refresh rate (Hz)
1～500	(mS) 14.4	69
1～800	24	41
1～1000	30	33

Table 7

If the system does not require a high data refresh rate, there is no requirement for the number of cascaded pixel arrays. As long as the power supply is normal, FW1906 can be used for unlimited cascading in theory.

2. How to make FW1906 work in the best constant current state



The output of FW1906 is a fixed constant current drive. According to the constant current curve, when the constant current is 18mA, the OUT voltage must be above 1.2V to enter the constant current area. Only then can the chip have a constant current effect. However, the higher the OUT voltage, the better. The higher the voltage, the greater the power consumption on the chip, the more serious the chip heating, and the lower the reliability of the entire system. Therefore, it is recommended that the voltage Vout be controlled between 1.2 and 3V when the OUT terminal is turned on. It is commonly used in series resistance. The following is the theoretical calculation method

for selecting resistance: System

drive voltage: VDD Single LED conduction

voltage drop: Vled Number of

series LEDs: n Constant

current value: Iout Constant

current voltage: 1.5V Resistance: R

$$R=(VDD-1.5-n\times Vled)/Iout$$

Example: System power supply 24V, single LED conduction voltage drop: 2V, number of series LEDs: 6, constant current value 18mA, according to the above formula,

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So: R = (24-2-2×6)/0.018 = 555Ω, just connect a 560Ω resistor in series to the OUT pin.

The resistance of R1-R6 can be adjusted according to the number of LEDs connected in series to the OUT port. It is recommended to connect 75-100 ohm resistors to R1 and R0. It is used for signal isolation to prevent the damage of the next-level chip from affecting the previous level.

RV is the IC voltage divider resistor, usually 1.2K for DC12V and 3K for DC24V. In addition, a power capacitor from 24V to GND should be added in the case of DC24V application.

5.1 To realize the chip to control the LED

brightness, first ensure that the RGB port voltage can make the chip enter constant current operation (for details, refer to "Constant Current"). flow curve").

5.2 The chip is powered on and reset. The port voltage reaches 1.2V. The output channel RGB has a fixed constant current of 18mA. The maximum current allowed to flow is

5.3 By changing the

PWM value continuously, you can adjust the LED brightness as you like. Set the PWM value to 0, the output is full high, and the LED is off. Set PWM

When the value is FFH, the output has the maximum low level duty cycle and the LED is the brightest.

Constant current curve

When FW1906 is applied to LED panel design, the current difference between channels and even between chips is extremely small. This is due to the excellent characteristics of FW1906. In

addition, when the load voltage changes, the stability of the output current is not affected, as shown in Figure 8. The FW1906 port drive current is a fixed constant current value.

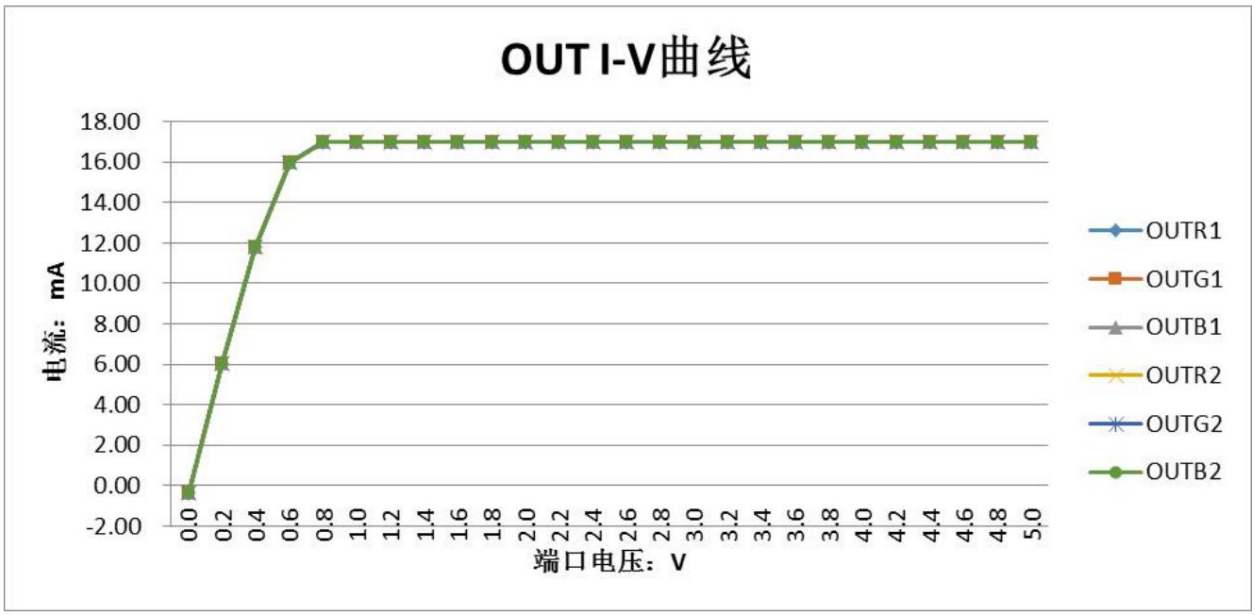

Fig. 9

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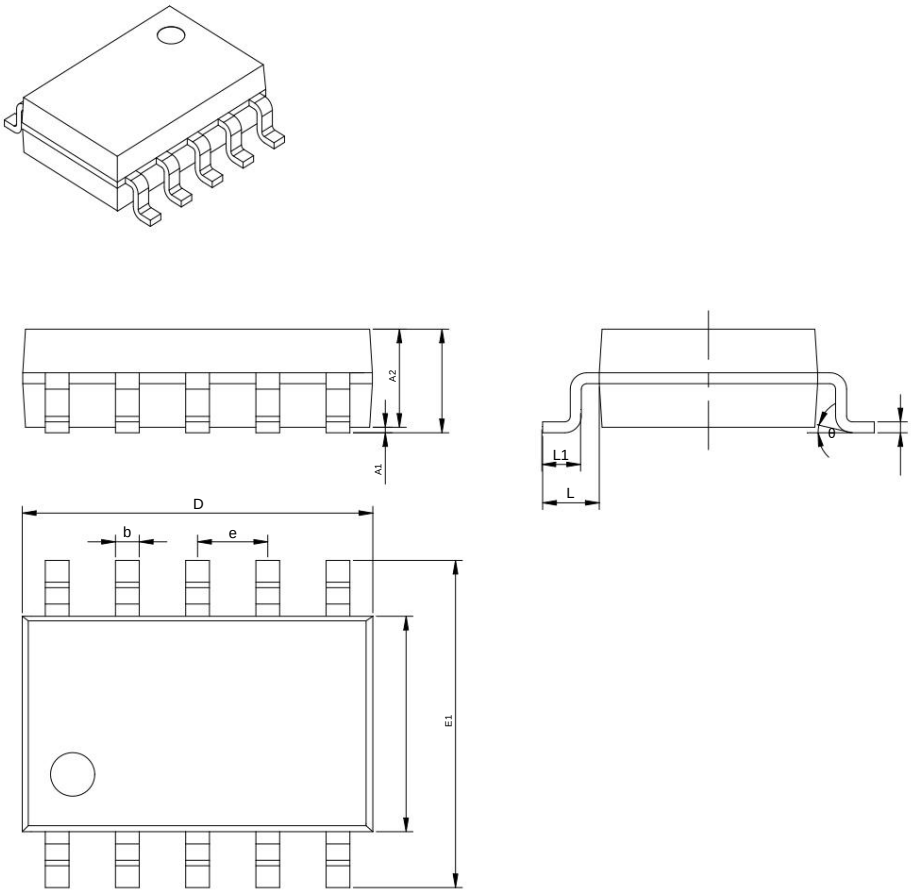
Package diagram (SSOP10)



Symbol	MSOP10				SSOP10			
	Dimensions In Millimeters		Dimensions In Inches		Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max	Min	Max	Min	Max
A	0.9	1.1	0.035	0.043	-	1.75	-	0.067
A1	0.05	0.15	0.002	0.006	0.10	0.225	0.004	0.009
A2	0.75	0.95	0.030	0.037	1.30	1.50	0.051	0.059
b	0.170	0.270	0.007	0.011	0.39	0.48	0.015	0.019
c	0.085	0.225	0.003	0.009	0.21	0.26	0.008	0.010
D	2.9	3.1	0.114	0.122	4.70	5.10	0.185	0.201
E	2.900	3.1	0.114	0.122	3.70	4.10	0.146	0.161
e	0.5(BSC)		0.020(BSC)		1.0(BSC)		0.039(BSC)	
E1	4.750	5.05	0.187	0.199	5.80	6.20	0.228	0.244
L1	0.4	0.6	0.016	0.024	0.50	0.80	0.197	0.032
L	0.95(BSC)		0.037(BSC)		1.05(BSC)		0.041(BSC)	
θ	0°	8°	0°	8°	0°	8°	0°	8°

All specs and applications shown above subject to change without prior notice.

(The above circuits and specifications are for reference only. If the company makes revisions, no further notice will be given.)

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